

What is claimed is:

1. A method for repairing an open gate line in an LCD, the LCD including a plurality of gate lines arranged on a substrate, a plurality of data lines that intersect with the gate lines to delineate a plurality of pixel areas, thin film switching transistors disposed proximate to gate line and data line intersections, and pixel electrodes disposed at the pixel areas, the method comprising the steps of:

when a gate line includes a gate open at an intersection with a data line, connecting that gate line with a first pixel electrode overlapping a portion of the gate line; and

connecting first and second adjacent pixel electrodes together across the gate open.

2. The repair method of claim 1, where the portion of the gate line and the pixel electrode overlap to form a storage capacitor, and wherein the gate line and the pixel electrode are electrically insulated by an insulating layer interposed between the gate line and the pixel electrode.

3. The repair method of claim 1, where the gate line includes a first side overlapped with the first pixel electrode and a second side overlapped with a second pixel electrode, and

where the step of connecting the gate line comprises the step of laser welding the first side to the first pixel electrode and laser welding the second side to the second pixel electrode.

4. The repair method of claim 3, where the first pixel electrode and the second pixel electrode are adjacent, and where the data line is disposed between the first pixel electrode and the second pixel electrode.

5. The repair method of claim 1, where the second pixel electrode is associated with the data line, and further comprising the step of electrically insulating the second pixel electrode from the data line.

6. The repair method of claim 5, where the step of electrically insulating comprises the step of disconnecting a drain electrode connected to the second pixel electrode.

7. A method for repairing an open gate line in an LCD, the LCD including a plurality of gate lines arranged on a substrate, a plurality of data lines that intersect perpendicular to the gate lines to delineate a plurality of pixel areas, thin film switching transistors disposed proximate to gate line and data line intersections, and pixel electrodes disposed at the

pixel areas, the method comprising the steps of:

when the gate line includes a gate open at a stepped intersection with a first data line, connecting together a first pixel electrode overlapped with a first predetermined portion of the gate line on a first side of the gate line;

connecting together a second pixel electrode overlapped with a second predetermined portion of the gate line on a second side of the gate line; and

connecting the first and second pixel electrodes.

8. The repair method of claim 7, where the first and second pixel electrodes overlap with the first and second predetermined portions to form storage capacitors.

9. The repair method of claim 7, where the step of connecting the first and second sides of the opened gate line comprises the step of welding the first and second sides.

10. The repair method of claim 7, where the first pixel electrode and the second pixel electrode are adjacent, and where the first data line is disposed between the first pixel electrode and the second pixel electrode.

11. The repair method of claim 7, where step of connecting

the first and second pixel electrodes comprises the step of depositing metal between predetermined portions of the first and second pixel electrodes.

12. The repair method of claim 11, where the step of depositing metal comprises the step of depositing the metal by laser chemical vapor deposition.

13. The repair method of claim 7, where the first data line is associated with the second pixel electrode, and where a second data line is associated with the first pixel electrode, and further comprising the step of electrically insulating the first data line from the second pixel electrode and electrically insulating the second data line from the first pixel electrode.

14. The repair method of claim 13, wherein the step of electrically insulating comprises the step of disconnecting a first drain electrode connected to the first pixel electrode and disconnecting a second drain electrode connected to the second pixel electrode.

15. A repaired display array substrate comprising:
an open gate line including a gate open, a first gate line portion on a first side of the gate open, and a second gate line

portion on a second side of the gate open; and

first and second pixel electrodes connected together and connected across the gate open.

16. The repaired display array substrate of claim 15, where the pixel electrodes are adjacent.

17. The repaired display array substrate of claim 15, where the gate open is disposed between the pixel electrodes.

18. The repaired display array substrate of claim 17, further comprising a data line that runs between the pixel electrodes and that intersects the open gate line at the gate open.

19. The repaired display array substrate of claim 15, further comprising a disconnected data line associated with the second pixel electrode.

20. A repaired display array substrate comprising:
gate lines intersecting with signal lines to delineate pixel areas in which pixel electrodes are disposed; where
the gate lines include an open gate line comprising:
a gate open;

a first gate line portion on a first side of the gate open, the first gate line portion overlapping a first one of the pixel electrodes; and

a second gate line portion on a second side of the gate open, the second gate line portion overlapping a second one of the pixel electrodes; and further comprising:

a first connection between the first gate line portion and the first pixel electrode;

a second connection between the second gate line portion and the second pixel electrode; and

a third connection between the first and second pixel electrodes.

21. The repaired display array substrate of claim 20, further comprising:

a disconnected transistor drain electrode coupled to at least one of the first and second pixel electrodes.

22. The repaired display array substrate of claim 20, further comprising:

a disconnected transistor source electrode coupled to at least one of the first and second pixel electrodes.

23. The repaired display array substrate of claim 20,

where the gate open is disposed beyond overlapping coverage of any single one of the pixel electrodes.

24. The repaired display array substrate of claim 20, where the gate open is disposed proximate to an intersection point between the open gate line and one of the data lines.

25. The repaired display array substrate of claim 20, where at least one of the first and second connections is a laser-CVD connection.

26. The repaired display array substrate of claim 20, where the third connection is a metal pattern formed between the first and second pixel electrodes.

27. A method for repairing a signal line with an open in an LCD, the method comprising the steps of:

connecting a first pixel electrode to a first side of the signal line;

connecting a second pixel electrode to a second side of the signal line; and

connecting the first pixel electrode to the second pixel electrode to establish a current path across the open.

28. The method of claim 27, where:

the step of connecting the first pixel electrode comprises the step of connecting a first pixel electrode that overlaps the signal line; and

the step of connecting the second pixel electrode comprises the step of connecting a second pixel electrode that overlaps the signal line.

29. The method of claim 27, where:

the step of connecting the first pixel electrode comprises the step of laser connecting; and

the step of connecting the second pixel electrode comprises the step of laser connecting.

30. The method of claim 27, where the step of connecting the first electrode to the second pixel electrode comprises the step of connecting adjacent first and second pixel electrodes.

31. The method of claim 27, where the step of connecting the first electrode to the second pixel electrode comprises the step of depositing metal between the first and second pixel electrodes.

32. The method of claim 27, further comprising the steps

of:

disconnecting a first data line from the first pixel electrode; and

disconnecting a second data line from the first pixel electrode.

33. The method of claim 27, further comprising the steps of:

disconnecting a first transistor drain electrode, associated with a first data line, from the first pixel electrode; and

disconnecting a second transistor drain electrode, associated with a second data line, from the second pixel electrode.